Roll No. ☐☐☐☐☐☐☐☐☐☐☐   Total No. of Pages : 02

Total No. of Questions : 18

B.Tech.(CSE)/(IT) (2012 to 2017)   (Sem.–3)
# DIGITAL CIRCUITS & LOGIC DESIGN
Subject Code : BTCS-303
M.Code : 56593

Time : 3 Hrs.   Max. Marks : 60

INSTRUCTION TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Answer briefly :

1) Perform 2's complement subtraction of $(7)_{10} - (11)_{10}$

2) What is race around condition? How it can be avoided?

3) How many states can an *n-bit* Ring counter and an *n-bit* Johnson's counter have?

4) What is meant by the term edge triggered?

5) How many flip-flops are required to design a mod-7 up down counter?

6) What is difference between static RAM and dynamic RAM?

7) What is EEPROM?

8) What are the advantages of ring counter?

9) Differentiate between A/D and D/A conversion techniques.

10) Write a short note on : SOP and POS.

SECTION-B

11) Prove the following identities using Boolean algebra :

$(A + B)(A + (AB)')C + A'(B + C') + A'B + ABC = C(A + B) + A'(B + C')$

12) A microprocessor uses RAM chips of 1024×1 capacity.

(a) How many chips will be required and how many address lines will be connected to provide capacity of 1024 bytes?

(b) How many chips will be required to obtain a memory of capacity of 16 K bytes?

13) What are the characteristics of digital ICs used to compute their performance?

14) Design an FPLA circuit, programed to implement a 3- bit binary to Gray conversion.

15) Design a sequence detector to detect the sequence **1010** (overlapping of the sequence is permitted). Use D flip-flop to design the circuit. Show the intermediate design steps :

   (a) State Diagram

   (b) Truth Table/ Excitation table

   (c) Logic Diagram of the circuit.

SECTION-C

16) A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations

   A is False, B is True

   A is False, C is True

   A, B, C are False

   A, B, C are True

   (a) Write the Truth table for F. Use the convention *True* = 1 and *False* = 0.

   (b) Write the simplified expression for F in SOP form.

   (c) Write the simplified expression for F in POS form.

   Draw logic circuit using minimum number of 2-input NAND gates.

17) Design a 8 to 1 multiplexer by using four variable function given by

   F (A, B, C, D) = $\square$m(0,1,3,4,8,9,15)

18) What are synchronous counters? Design a 3-bit Gray code counter using T-Flip Flop.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.